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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,451	08/27/2003	Subhas C. Bose Jayappa Veeramma	011775-013210US	7137

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

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06/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/650,451	BOSE JAYAPPA VEERAMMA ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-3 and 26-30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The claimed limitations of "a peripheral junction region of second conductivity formed at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, the peripheral junction region being configured to float electrically" mean that one possible structure of the recited claim is that the peripheral junction region extends beyond the boundaries of the isolation diffusion region. In this situation the peripheral junction region is not electrically floating. Therefore, there is no support in the embodiment of figures 3-4 and 6 for the claimed limitations of "a peripheral junction region of second conductivity formed at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, the peripheral junction region being configured to float electrically", as recited in claim 1.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-3 and 26-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of "a peripheral junction region of second conductivity formed at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, the peripheral junction region being configured to float electrically", as recited in claim 1, are unclear as to whether the peripheral junction region is electrically floating, or the peripheral junction region extends beyond the boundaries of the isolation diffusion region, and thus is not electrically floating.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 25-26, 28 and 30, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yano (5,138,415) in view of Gross (5,316,964).

Yano teaches in figure 2 and related text a power device, comprising:

a semiconductor substrate 16 of first conductivity having an upper surface and a lower surface;

a first electrode terminal 29 coupled to a first conductive region 24 provided proximate the upper surface of the substrate, the first electrode terminal being provided over the upper surface of the substrate;

a second electrode terminal 36 coupled to a second conductive region 18 provided proximate the lower surface of the substrate, the second electrode terminal being provided below the lower surface of the substrate;

an isolation diffusion region 17 of second conductivity P provided at a periphery of the substrate and extending from the upper surface to the lower surface of the substrate, the isolation diffusion region having a first surface corresponding to the upper surface of the substrate and a second surface corresponding to the lower surface; and

a passivation layer 28 provided over the upper surface of the substrate, the first surface of the isolation diffusion region;

wherein the first and second electrode terminals define a vertical electrical current path there between, and

wherein the peripheral junction region is provided to compensate the surface depletion of the isolation diffusion region.

Yano does not teach a peripheral junction region of second conductivity formed at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, wherein the peripheral junction region being configured to float

electrically, and wherein the peripheral junction region is different than the first and second conductive regions.

Gross teaches in figure 2 and related text a peripheral junction region 24 of second conductivity N+ formed at least partly within an N type isolation diffusion region 16, 17 and formed proximate the first surface of the isolation diffusion region, wherein the peripheral junction region being configured to float electrically.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a peripheral junction region of second conductivity at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, wherein the peripheral junction region being configured to float electrically, in Yano's device in order to increase the electrical isolation of the device. The combination is motivated by the teachings of Gross who points out the advantages of using a peripheral junction region within the isolation junction region (column 2, lines 39-41).

Note that prior art's device includes a peripheral junction region being different than the first and second conductive regions.

Regarding claims 26, 28 and 30, prior art's device includes a passivation layer includes an oxide layer and contacts the upper surface of the substrate, the first surface of the isolation diffusion region, and the peripheral junction region,

wherein the peripheral junction region is provided to compensate the surface depletion of dopants in the isolation diffusion region and increase a reverse blocking

voltage of the device by reducing an electric field at the first surface of the isolation diffusion region, and

wherein the device is a diode and the first electrode terminal being separated from the isolation diffusion region.

Claims 27 and 29, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yano and Gross, as applied to claims 1 and 26 above, and further in view of Collins (5,262,754).

Yano and Gross teach substantially the entire claimed structure, as applied to claims 1 and 26 above, except a passivation layer includes a polymid layer over the oxide layer. Collins teaches using a polymid layer when packaging the device (column 2, lines 50-55).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a polymid layer when packaging the device, such that the passivation layer includes a polymid layer over the oxide layer, in prior art's device in order to provide better protection for the device.

Response to Arguments

Applicant's arguments with respect to claims 1-3 and 26-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference D is cited as being related to isolation regions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
6/10/07

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